AMENDMENTS TO THE SPECIFICATION

Please amend the second paragraph on page 3 as follows:

As a result, the area in which the capacitor is formed is decreased but height of the capacitor is ~~heightened~~increased. So, it is difficult to form the stable bottom electrode and especially there ~~is~~ occur~~reds~~ ~~some~~a critical problem because of neighboring bottom electrodes which are connected to each other.

Please amend the third paragraph on page 3 as follows:

In addition, because cylinder type capacitor can use at inside and outside of the bottom electrode, the area in which a charge is stored ~~broaden twice~~increased two-fold and the predetermined capacitance is easily obtained. However, ~~at~~after removing the sacrificial layer 14 for making the outside of the bottom electrode usable, the capacitor may be connected to another capacitor because of an insufficient space of the bottom electrode.

Please amend the fifth paragraph on page 3 (continued on page 4) as follows:

As shown, when the sacrificiale layer is removed after the bottom electrode is formed inside the trench, an error is occurred because of the connecting of the bottom electrodes to each other. (referred as A area)

Please amend the third paragraph on page 4 as follows:

As shown in Fig. 3A, the inter-insulation film 12 is formed on the substrate 10 where the active area 11 is formed. The contact trench is formed to connect to the active area 11 in the substrate 10 by penetrating the inter-insulation film 12. The contact plug 13 is formed by filling the conductive material. Then, the first and second sacrificiale films 19 and 20 are formed in size of the capacitor. The first sacrificial film 19 is made of a phosphor-silicate glass layer (hereinafter, referred as PSG), and the second sacrificial film for capacitor 20 is made of the tetraethylorthosilicate layer (hereinafter, referred as TEOS).

Please amend the fifth paragraph on page 4 (continuing on page 5) as follows:

The trench 21 is formed by either wet etching process once or additionally etching the second sacrificiale layer 20 in the manner of wet etching process, after the first and the second sacrificiale layer 19 and 20 are selectively etched in the manner of dry etching process.

Please amend the second paragraph on page 5 as follows:

As shown in Fig. 3B, the first and second sacrificiale layers 19 and 20 are eliminated. The dielectric thin layer 23 is formed on the bottom electrode 22. The top electrode 24 is formed on the dielectric thin layer 23.

Please amend the sixth paragraph on page 5 (continuing on page 6) as follows:

In addition, because the PSG layer used as the first sacrificiale layer has a characteristic of absorbing water, there is pointed the problem that the hill is generated in upper part of the trench by increasing volume of the PSG layer at the wet etching process which forms the trench. Namely, according to use the PSG layer as the first sacrificial layer, the upper surface of the TEOS layer used as the second sacrificial layer is not even after all process is completed. If the bottom electrode is made by using the uneven hole for capacitor, it is not possible to produce the bottom electrode which has a stable shape.

Please amend the fourth paragraph on page 6 as follows:

In accordance with an aspect of the present invention, there is provided the method for fabricating the capacitor for a semiconductor device including the step of: forming a sacrificial layer in the height of capacitor on the substrate so that a etch rate becomes lower if it's height becomes higher; forming a trench by selectively eliminating the sacrificiale layer in manner of wet etch process; forming a bottom electrode in the trench; eliminating the sacrificial layer; forming a dielectric thin film on the bottom electrode; and forming the top electrode on the dielectric thin film.

Please amend the first paragraph on page 8 as follows:

Fig. 7 is a table composed of several graphs presenting a wet etch rate and a deposition rate of a TEOS layer in response to process conditions.

Please amend the second paragraph on page 9 as follows:

If ~~there is occurred~~ a variation of the process occurs when the sacrificiale layer is formed by the plasma enhanced CVD, the sacrificiale layer is deposited by controlling the etching select ratio, but, in the present embodiment, the TEDS layer is used at the process.

Please amend the third paragraph on page 9 as follows:

Fig. 7 is a table which is composed of several graphs presenting a wet etch rate and a deposition rate of a TEDS layer in response to process conditions. As shown, the wet etch rate is varied in response to a RF power, an 0_2 flow, a spacing between the substrate and the shower head.

Please amend the fifth paragraph on page 9 (continuing on page 10) as follows:

Thus, when the TEDS layer used as the sacrificiale layer 34 is formed, the first TEDS layer 34a is formed by controlling the process condition so that it's wet etch rate is high, and the second TEOS layer 34b is formed so that it's wet etch rate is low. Then, if the trench is formed, lower part of the trench is wide and upper part of the trench is narrow.

Please amend the second paragraph on page 10 as follows:

In addition, if the sacrificiale layer 34 is deposited by at least three steps, the deposited TEOS layer can be deposited so that it's wet etch rate is diversified.

Please amend the fifth paragraph on page 10 (continuing on page 11) as follows:

If the capacitor is produced by the above described manner, the capacitor is more stably formed by using one TEOS layer when it is compared with the capacitor

which has the sacrificiale layer formed by two processes using the PSG and TEOS layers according to the prior art. In addition, the hill is not generated because the PSG layer which generates the hill by absorbing water at the wet etching process is not used at the process.

IN THE ABSTRACT

Please replace the current abstract with the following new abstract. The abstract is also enclosed on a separate sheet.

A method of fabricating a capacitor for improving the shape of a bottom electrode by using a sacrificial layer at a producing process. The method includes forming a sacrificial layer in the height of the capacitor on a substrate, an etch rate of an upper portion of the sacrificial layer is lower than that of a lower portion of the sacrificial layer, and the sacrificial layer is a TEOS layer; forming a trench by selectively eliminating the sacrificial layer by a wet etch process; forming a bottom electrode in the trench; eliminating the sacrificial layer; forming a dielectric thin film on the bottom electrode; and forming the top electrode on the dielectric thin film.